EXHIBIT D

DECLARATION OF GARY JAMES EWELL

1. I am Gary James Ewell. My Curriculum Vitae is attached as Exhibit 1 to this document. I have been retained by Presidio Components, Inc. ("Presidio") as a technical consultant and expert witness in this case. My declaration is based upon my own personal knowledge and experience.

2. The patent in suit, U.S. Patent No 6,816,356 (the '356 Patent), relates generally to multilayer capacitors, which are formed from multiple layers of conductive and dielectric (non-conductive) materials. I am an expert in this field with multiple, related publications and presentations and was recognized as such by the then National Research Council of the National Academy of Sciences, through an invitation to be a presenter at their 1982 Workshop on "The Reliability of Multilayer Ceramic Capacitors", held March 29-31, 1982 in Washington, D.C.

3. I have been asked to do the following. To read the '356 Patent and the associated papers in this case and as one sufficiently skilled and experienced in the art of designing and manufacturing reliable Multilayer Capacitors to come to conclusions as to the definiteness of certain terms used in the claims of the '356 Patent that are in question. By definite I mean that I and others would understand and have a clear technical picture of what is being claimed and believe that one skilled in the art at the time the patent application that issued as the '356 patent was filed, as defined by Dr. J. P. Dougherty, would be able to understand and arrive at a specific and usable design.

4. Materials used for this declaration. First, the documents supplied by legal counsel, are following:

-U.S. Patent No. 6,816,356 B2
-ATC's Memorandum of Points and Authorities in Support of Its Motion for Summary Judgment of Indefiniteness
-Claim Construction Order
-Document Set PCI 00001 - PCI 00013
-Document Set PCI 00057 - PCI 00161
-Document Set PCI 00300 - PCI 00377
-Joint Claim Construction Chart, Worksheet and Hearing Statement
-Presidio Components, Inc.'s Brief on Claim Construction
-Presidio Components, Inc.'s Responsive Brief on Claim Construction

Second, my own personal library of patents, US and foreign, technical articles, notes, and books. Third, my notes as a technical auditor for the US Government, Defense Supply Center, Columbus, Ohio, ('DSCC') of a large number of US Manufacturers attempting to qualify for and deliver product to US Military Specifications for a Variety of Multilayer Ceramic Capacitor styles and configurations.

5. First Term of "substantially monolithic". My understanding is that the Court has defined the term as "a dielectric body largely but not wholly without seams from the inclusion of plates within the dielectric body".

6. It is my opinion that the term above, as defined by the Court, is clear and understandable as used in the '356 Patent to one of ordinary skill in the art, as defined by Dr. J. P. Dougherty, at the time the patent application that issued as the '356 patent was filed. The reasons why I hold this opinion follow. First, the '356 Patent's claims do involve one or more capacitor constructions within a single dielectric body, wherein each construction contains as a minimum two conductive contacts and a dielectric material located in between; this is a standard definition and that the dielectric body containing such constructions is to be sufficiently sintered, fused, or joined as to constitute a

single monolithic structure is understood. Second, such internal voids or gaps remaining within the dielectric body after fusing or sintering or joining would not detract from the physical integrity or "monolithicity" of the structure, in terms of its ability to resist fracturing when subjected to the normal range of forces involved in placing the component on a substrate and then to normal subsequent thermo mechanical stresses involved in its application by a user; such requirements for capacitors are normal and expected, in my opinion.

7. In my opinion the technical reasons why the claim put forth by American Technical Ceramics ("ATC"), that the First Term is unclear or indefinite, is incorrect follow. First, the use of the term is definite and specific in that it refers to a monolithic body with possible more voids and seams than is normal in a simple, sintered monolithic "chip" or "brick" configuration. This is to be expected as this array of capacitors can involve the sintering together of an array or grouping of such individual "chips". Second, the degree of additional voids and seams will vary from configuration to configuration so that the term "substantially" cannot be given a single definition in terms of percent of theoretical density; that percentage will vary from design to design and from manufacturing "run" to manufacturing "run". The varying amount of voids, gaps, and seams that would occur in capacitors would seem to make use of the technical term "substantially" very appropriate in this situation. Third, one of ordinary skill in the art, as defined by Dr. J. P. Dougherty, would refer to individual "chips" or "bricks" as monolithic. When multiples of these "chips" or "bricks" are sintered together into a single body, it would be understood by one skilled in

the art, at the time the patent application that issued as the '356 patent was filed, that the resultant array or grouping also would be considered as monolithic, but to a lesser degree than just a single "chip". The use of the phrase "substantially monolithic" then would be understandable to one wanting to differentiate between the amount of voids, gaps, and seams expected in a single "chip" and the amount of voids, gaps, and seams expected in an array of chips sintered into a single, more-complex body.

8. In my opinion there is an objective standard that one skilled in the art, at the time the patent application that issued as the '356 patent was filed, would use for determining whether a particular dielectric body or sintered array of dielectric bodies is "substantially monolithic" or not. One would manufacture samples of a particular design and put them through the normal manufacturing and testing sequence and then additionally put them through a higher-level electronic hardware assembly sequence designed to envelope those assembly sequences of the typical device users. This sequence might involve part placement on a substrate, attachment by soldering, cleaning of the soldered joint, electrical testing of the completed substrate and finally exposure of the completed substrate to a range of environment conditions, including extremes in temperature exposure and high humidity. If the internal gaps, voids, and seams are so small or minor within the parts that the samples remain integral under those conditions and do not fragment or break into pieces, then the body would be considered "substantially monolithic". If the samples did

fragment or shatter, than the body would not be considered "substantially monolithic".

9. Fourth Term of "The Second Contact Being Located Sufficiently Close To the First Contact to Form a First Fringe-Effect Capacitance with the First Contact". It is my understanding that the Court has defined the term as "an end of the first conductive contact and an end of the second conductive contact are positioned in an edge-to-edge relationship in such proximity as to form a determinable capacitance".

10. It is my opinion that the Fourth Term above, as defined by the Court, is clear and understandable as used in the '356 Patent to one of ordinary skill in the art of designing and manufacturing such multilayer dielectric capacitors, as defined by Dr. J. P. Dougherty, at the time the patent application that issued as the '356 patent was filed. The reasons why I hold this opinion follow. First, the words used in the '356 Patent and its associated Figures involve use of such "fringe-effect capacitors" as built into the networked array of capacitors to allow tailoring and adjustment of the capacitor's behavior at high frequencies, as described in the '356 Patent. Second, I am of the opinion that such "fringe-effect capacitors" involving edge to edge electrical conductor electrical relationships have already been used in the capacitor industry, in single chip configurations, and thus reference to them would be clear and definitive for a capacitor designer who would be able to consider those designs either in his/her company's design guidelines or in those manufactured elsewhere.

11. In my opinion the reasons why the argument put forth by American Technical Ceramics ("ATC"), that the Fourth Term is unclear or

indefinite, is incorrect follow. First, it is not the degree of spacing between the two edge-to-edge conductors that is directly significant, but the capacitance that is formed between them, its variation at high frequencies, and the affect on insertion loss of the entire array. Second, the amount of capacitance formed and its behavior over frequency will also vary by the exact location of the conductors on the external surface of the "substantially monolithic" array body, as other conductors at a further distance and the specific nature of the underlying dielectric material will affect the properties of the specific "fringe-effect capacitor". Third, it is my opinion that the Claims involved in the '356 Patent for "fringe-effect capacitors" are unique in that they involved the networked array of such capacitors in conjunction with multilayer capacitors in a single, "substantially monolithic" body and that the adjustment of those capacitors to arrive at a final capacitance value and behavior for the array is new for the '356 Patent, not achieving a precise value for any given "fringe-effect capacitor". Fourth, in my opinion the Term "A First Fringe-Effect Capacitance" is sufficiently definite for a designer, as the word "First" would be readily understood as relating to the first of an arbitrary numbering of multiple fringe-effect capacitors along the surface of the monolithic array of capacitors, the numbering scheme relating to which particular fringe-effect capacitor is designated "one" or "first", which one designated "two" or second, etc. One of ordinary skill in the art would not understand there to be multiple fringe-effect capacitances between the same two contacts at the same location. It would be understood that a single, "first," fringe-effect capacitance is between the two contacts at the same location.

12. In my opinion there in an objective, workable standard that one skilled in the art, at the time the patent application that issued as the '356 patent was filed, would use for determining whether a particular "fringe-effect capacitor", designed per the above definition, was determinable. One of ordinary skill in the art, as defined by Dr. Dougherty, would be able to make that determination through detailed electrical testing of samples of each member of a family of similar array designs. In general terms, this is how that would happen. One would manufacture samples of each of a family of array designs, each design varying the strength of the "fringe-effect capacitor" by varying the spacing of the external surface conductors forming the capacitor. One would then electrically measure the properties of the various groups of samples and then associate the change in electrical properties, affect on insertion loss, and affect on data loss, from group to group with the variation in the design of the fringe-effect capacitor. If the capacitor change resulted in a specific change in array electrical properties, then it would be determinable.

13. In my opinion, one of the novel claims of the '356 Patent is to use such fringe-effect capacitors within an array of capacitor elements. This use allows the tailoring of the electrical properties of the overall array to meet specific requirements. No more will a user have to add individual, fringe-effect or other capacitors designed for high-frequency behavior as discrete parts to his/her circuit, but will

be able to purchase them as integral to a capacitor array designed just for his application. The capacitor user will thus save on space, weight, and any reliability losses that are associated with having to interconnect an additional discrete part.

14. Fifth Term of "The Second Contact Being Located Sufficiently Close to the First Contact on the Second Side of the Dielectric Body to Form a Second Fringe-Effect Capacitance with the First Contact". It is my understanding that the Court has defined the term as "another end of the first conductive contact and another end of the second conductive contact are present on the second side of the substantially monolithic dielectric body and are positioned in an edge-to-edge relationship in such proximity as to form a determinable capacitance."

15. It is my opinion that the Fifth Term above, as defined by the Court, is clear and technically understandable as used in the '356 Patent to one of ordinary skill in the art of designing and manufacturing such capacitors, as defined by Dr. J. P. Dougherty, at the time the patent application that issued as the '356 patent was filed. The reasons why I hold this opinion follow. First, in a manner similar to that described above, such "fringe-effect capacitors", no matter where they are located on the surface of the substantially monolithic body, will have a capacitance that, if significant in magnitude to other capacitor constructions within the networked array of capacitors, will contribute to the overall response of the array in its application and thus will allow for tailoring of that response by adjustment of capacitor properties, such as spacing of the contacts and location with respect to other capacitors in the array. Second, such

electrical contacts are normally present on the very great majority of multilayer dielectric capacitors, as a consequence of the manufacturing process involving dipping and firing of the external conductive materials, but not used to form a fringe-effect capacitor, and it is one of the unique advances of this '356 Patent to decrease the normal spacing between such contacts to the point where they form a determinable and useable fringe capacitance that can then be used to adjust high frequency responses of the capacitor array.

16. In my opinion the reasons why the claim, put forth by American Technical Ceramics ("ATC"), that the Term above is unclear and indefinite, is incorrect follow. First, it is not the degree of spacing between the two edge-to-edge conductors that is directly significant, but the capacitance formed between them and the behavior of that capacitance at high frequencies that is of importance to the designer. Second, the amount of capacitance formed and its behavior over frequency will also vary by the exact location of the conductors along the surface of the "substantially monolithic" body, whether on the First or Second Side of the dielectric body, as other conductors at a further distance and the nature of surrounding dielectric materials may affect the electrical properties of the specific "fringe-effect capacitor" of interest.

17. Sixth Term of "the dielectric body has a hexahedron shape". It is my understanding that the Court has defined the term as "the substantially monolithic dielectric body has six sides".

18. With the term as defined above, the '356 Patent covers bodies having at least six sides; in many of the examples presented in the

'356 Patent, the articles in question have more than six sides, although the additional sides appear relatively quite small in area and this contributing little to overall device capacitance. Based on that information it is my opinion that the term above, as defined by the Court, is clear and understandable as used in the '356 Patent to one of ordinary skill in the art of multilayer capacitor design, as defined by Dr Dougherty, at the time the patent application that issued as the '356 patent was filed. The reasons why I hold this opinion follow. First, all of the US-manufactured monolithic dielectric bodies that are commercially available, that I am aware of have, at least six sides. Second, none of the US-manufactured multilayer dielectric capacitors that I am familiar with have only six sides in an extremely precise sense; they usually have very minor additional sides formed by the surfaces of external conductive layers as they are fused to the dielectric body or by small, surface defects, such as "chip outs" or "spalls" in the body that may or may not be covered by the external conductive layers.

19. In my opinion the reasons why the claim put forth by American Technical Ceramics ("ATC") that the Sixth Term above is unclear and indefinite is incorrect follow. First, current US-manufactured multilayer dielectric capacitors have at least six major sides. They can be considered to have additional sides if minor imperfections or if deliberate modifications, such as leads added to a capacitor body, are considered. Such leads or imperfections appear not to be considered by the ATC's claim of indefiniteness. Second, I consider the six sides in standard monolithic dielectric capacitors to be "major" in that they

contribute the very great majority of capacitance to the capacitor array and were designed to do so. Third, in my opinion it is entirely feasible and technically possible to design a "substantially monolithic dielectric body" with more than six major or significant sides.

20. In my opinion, one of ordinary skill in the art, as defined by Dr. J. P. Dougherty, would immediately understand that the phrase "the ceramic body" in Claim 18 of the '356 Patent is referring to the phrase "substantially monolithic dielectric body" in Claim 1 of the '356 Patent. The reasons for my opinion follow. First, many writers of technical papers and of Capacitor Handbooks use the terms interchangeably, given the context of describing multilayer ceramic manufacturers, where ceramic is understood to be the dielectric in the capacitor design. Second, manufacturers of ceramic powders for the multilayer ceramic capacitor industry sell those powders as "dielectrics", emphasizing that their electrical properties, as opposed to chemical or mechanical properties, are the key reason for their purchase.

21. I am being compensated at the rate of $200 per hour for the work in creating this Declaration.

I declare and verify under penalty of perjury that the foregoing is true and correct.

Dated this 11 day of July, 2008

Gary James Ewell

Dr. Gary J. Ewell

Consultant

Years Technical Experience: 45

Special Qualifications

Gary Ewell received a B. S. Materials Science degree from Stanford University, California, in 1963, followed by an M.S. Materials Science in 1964 and Sc.D. in Metallurgy in 1968 from the Massachusetts Institute of Technology. He worked as a research engineer at NASA, Ames Research Center, and was a visiting Professor at the Universidad Technica del Estado in Santiago, Chile, and worked at Hughes Aircraft Company. He joined The Aerospace Corporation and retired after 24 years of service.

His industry positions allowed him to support various satellite and launch vehicle Program Offices, as well as interface with other government (e.g., NASA, DLA/DSCC, JPL, etc.) and industry organizations (e.g., ISO 9000 certification firms, OEMs) providing reliability, risk management, configuration management, and quality engineering specialists and tools in order to resolve hardware and software issues.

Gary has authored and co-authored more than 40 papers and presentations on reliability, passive components, failure analysis, Risk Management, and other topics presented at various USA, European, and Asian conferences. He has been a consultant for the National Science Foundation and has participated in NATO Advanced Research Workshops.

Work Experience

- **The Aerospace Corporation (1983 to 2007)**

Director, Quality & Reliability Department and Senior Staff Specialist. Duties have involved all aspects of reliability, risk assessment, manufacturing readiness, quality assurance, and ISO 9000 activities.

Other experience includes:

- Panel lead, Independent Assessment Teams for International Space Station
- Co-Heads External Review Team for NASA - GSFC on GOES Mission
- Member Independent Assessment Team for SIR-B and Cassini missions at JPL
- Specialist in reliability of electronic components
- Member Technical Planning Committee for Aerospace/USAF 2nd and 3rd Risk Management Conferences

Education:

- BS, Materials Science - Stanford University, 1963
- MS, Materials Science - Stanford University, 1964
- Sc. D., Metallurgy - Massachusetts Institute of Technology, 1968
- MA, History - University of Santa Clara

Professional Societies, Honors, Awards

- Member Program Committee IEEE Components Conference and Member Program Committee IEEE/CTI Capacitor and Resistor Technology Symposium Conferences
- Winner, Best of Conference Paper awards three times.

Expert Witness Experience

- 1985 - 86, Technicare vs. Centralab & CAM Ohio Electronics, Court unknown
- 1992 - 93, Liebert Corporation vs. North American Philips Corporation, Superior Court of California in the County of Orange

Publications

- Over 40 publications pertaining to statistical quality control, quality auditing, failure analysis, and capacitors.

Partial List follows, some with coauthors.

- "Adhesion Degradation of Soldered Thick Film Chip Resistors During Elevated Temperature Exposure", Proceedings International Microelectronics Symposium (ISHM), 1975, pp. 168-177.
- "Application of Advanced Failure Analysis Techniques to Practical Aerospace Problems", Proceedings, SAMPE, 1976.
- "Materials Incompatibility of Multilayer Ceramic Chip Capacitors", Proceedings, International Microelectronics Symposium (ISHM), 1976.
- "Metallurgical Criteria for Selection of Solders for Micro-electronic Uses", Proceedings, International Microelectronics Symposium (ISHM), 1976, pp. 239-248.
- "Reliability of Printed Wiring Board Solder Interconnections/Passive Devices", Proceedings NEPCON, Anaheim, CA., 1976, pp. 265-273.
- "Reliability Problems in Reflow Soldering Ag and Pd-Ag Terminated Chip Components", Proceedings Electronics Components Conference, 1977, pp. 206-211.
- "Encapsulation, Sectioning, and Examination of Multilayer Monolithic Chip Capacitors", Proceedings Electronic Components Conference, Arlington, 1977, pp. 446-451.
- "Heat Pipe Materials", Proceedings SAMPE, 1977.
- "Heat Pipes for Hostile Environments in Energy Conservation Applications", Proceedings 12th Intersociety Energy Conversion Engineering Conference, 1977.
- "Special Lot Acceptance Tests for Multilayer Ceramic Capacitors", Proceedings Electronic Components Conference, Arlington, 1977, pp. 452-257.
- "The Piezoelectric Properties of Multilayer Ceramic Capacitors", Proceedings International Microelectronics Symposium (ISHM), 1977.
- "Adhesion Measurements of Thick Film, Glass-Fritted Inks on Chip Components", Adhesion Measurement of Thin Films, Thick Films, and Bulk Coatings, ASTM STP No. 640, ASTM, Philadelphia, 1978, pp. 251-268.
- "Acoustic Microscopy of Ceramic Capacitors", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. CHMT-1 (3), Sept. 1978, pp. 251-257.
- "Low Cost Liquid - Metal Heat Pipes", Proceedings 3 International Heat Pipe Symposium, 1978.
- "Material Incompatibilities in Ceramic Chip Capacitors", Inter. Journal Hybrid Microelectronics, Vol. 1 (2), July, 1978, pp. 77-86.
- "Non-Destructive Examination of Multilayer Capacitors by Neutron Radiography", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. CHMT-1 (3), Sept. 1978, pp. 265-273.
- "A Fracture Mechanics Approach to Structural Reliability of Ceramic Capacitors", IEEE Transactions of Components, Hybrids, and Manufacturing Technology, Vol. CHMT-3 (2), June 1980, pp. 250-257.
- "A Cause of the Non-Solderability of Ceramic Capacitor Terminations", Capacitor Technologies, Applications and Reliability, NASA - CP -2186, June 1981, pp. 99-105.
- "Chemical and Microstructural Analyses of Grain Boundaries in $BaTi0_3$ - based dielectrics", Grain Boundary Phenomena in Electronic Ceramics, ed. L. M. Levinson, American Ceramic Society, Columbus, OH, 1981, pp. 207-214.
- "Solder Coating of Ceramic Capacitors: Wettability Problems", Proceedings International Society of Testing and Failure Analysis (ISTFA), Los Angeles, 1981, pp. 111-116.
- "Electrical Analysis of Capacitors Failing the 85°C/85%/RH/1.5VDC Test", Proceedings 2nd Capacitor and Resistor Technology Symposium (CARTS), New Orleans, 1982, pp. E1-1 to E1-12.

- "Solder Coating of Ceramic Capacitors: Wettability Problems", Proceedings International Society of Testing and Failure Analysis (ISTFA), Los Angeles, 1981, pp. 111-116.

- "Electrical Analysis of Capacitors Failing the 85C/85%RH/1.5 VDC Testing", Proceedings 2nd Capacitors and Resistor Technology Symposium (CARTS), New Orleans, 1982, pp. E1-1 to E1-12.

- "Extended Electrical Characterization of Ceramic Capacitors Failing Under Low-Voltage Conditions", Proceedings International Society of Testing and Failure Analysis (ISTFA), San Jose, CA 1982, pp. 194-202.

- "Multilayer Capacitor Reliability: How Significant are Physical Defects?", Proceedings National Academy of Science Workshop on Reliability of Multilayer Ceramic Capacitors, 1982, Washington, D. C.

- "The 85°C-85% Relative Humidity - 1.5 VDC Bias Test: Can Ceramic Capacitors Pass This New Screen?, Proceedings 3rd Capacitors and Resistor Technology Symposium (CARTS), Phoenix, AZ, 1983, pp. 70 -77.

- "Reverse Bias Characteristics of Solid Tantalum Capacitors", Proceedings 4th Capacitor and Resistor Technology Symposium (CARTS), 1984, pp. 21-29.

- "Sweep Voltammetry: A new Tool for Capacitor Characterization: Proceedings 5th Capacitor and Resistor Technology Symposium (CARTS), 1985, pp. 94-113.

- "High Frequency Ultrasonic Properties of Ceramic Capacitors", Proceedings 5th Capacitor and Resistor Technology Symposium (CARTS), 1986.

- Microstructure of High-Fired NPO Ceramic Capacitors", Proceedings 6th Capacitor and Resistor Technology Symposium (CARTS), 1986, pp. 7-13.

- "Low Voltage Insulation Resistance Failures in Multilayer Ceramic Capacitors", Proceedings 1st European Capacitor and Resistor Technology Symposium (CARTS), 1987. pp. 125.

- "Space Quality Resistors and Capacitors: Where We Are and Where We Are Going", Proceedings 6th Capacitors and Resistor Technology Symposium (CARTS), 1987, pp. 19.

- "Critical Mechanical Properties of Ceramic Chip Capacitors", Proceedings 2nd European Capacitor and Resistor Technology Symposium (CARTS-Europe), 1988.

- "Ceramic Processing Effects on the Piezoelectric Behavior of MLC Capacitors", Proceedings 2nd European Capacitor and Resistor Technology Symposium (CARTS), 1989, pp. 67-71.

- "Controlling Cracking in Ceramic Capacitors: A Fracture Toughness Approach, Proceedings SMART V, New Orleans, LA, 1989.

- "Laminate Bond Strength Test: A New Quality Tool for Ceramic Capacitors", Proceedings Expo SMT 1990, 1990, pp. 523-528.

- "Methods of Characterizing Cast Tape for Multilayer Ceramic Capacitors", Proceedings 10th Capacitor and Resistor Technology Symposium (CARTS), 1991, pp. 183-203.

- "Space Quality Capacitors, Resistors and EMI Filters: Achievements, Progress and Concerns", Proceedings 10th Capacitor and Resistor Technology Symposium (CARTS), 1991, pp. 147-151.

- "TQM, SPC, and PPM Practices for Passive Components", Proceedings 1st Asian Capacitor and Resistor Technology Symposium (CARTS-ASIA), 1991, pp. 128-142.

- "Effects of Vacuum, Moisture Exposure, and Polarity Reversal on the Resistance Drift Rate of Philips Nonhermetic Metal Film Resistors", Proceedings 11th Capacitor and Resistor Technology SymposiuSymposium (CARTS

- "Effects of Vacuum Moisture Exposure, and Polarity Reversal on the Resistance Drift Rate of Philips Nonhermetic Metal Film Resistors", Proceedings 11th Capacitor and Resistor Technology Symposium (CARTS), 1992, pp. 218.

- "Design and Construction of Precision Resistors", Capacitor and Resistor Technological Symposium, 1995
- "Space-Quality Capacitors, Resistors, and EMI/RF Filters", Electronics Technology and Microtechnology, 1996
- "Precision Resistors: A State of the Art Review", Nepcon '96
- "Development of Pb-Free Solders: An Overview", International Symposium Electronic Packaging Technology (ISEPT), Shanghai, P. R. China, 1996
- "Current Trends and Future Issues in Solderability", ISHM/NATO Advanced Research Workshop on Microelectronic Interconnections and Microassembly, Czech Technical University, Prague, Czech Republic, 1996
- "Space-Quality Capacitors, Resistors, and EMI/RF Filters", Proceedings Capacitor and Resistor Technology Symposium (CARTS), 1997
- "New Approaches to Preserving Solderability on PSBs", Proceedings, NEPCON West, 1997
- "Stacked Capacitors: A User's Guide", Proceedings Capacitor and Resistor Technology Symposium (CARTS), 1998
- "Tin Whiskers and Passive Components: A Review of the Concerns", Proceedings Capacitor and Resistor Technology Symposium (CARTS), 1998
- "Solid TA Capacitors: Polymer vs Manganeous Oxide Electrolytes - A Review", ,Proceedings Capacitor and Resistor Technology Symposium (CARTS), 2000, pp. 39 - 46.
- "Measuring The Mechanical Properties of Multilayer Ceramic Capacitors, Proceedings Capacitor and Resistor Technology Symposium (CARTS), 2000, pp. 162 - 172.
- "Third Harmonic Testing: An Initial Review", , Proceedings Capacitor and Resistor Technology Symposium (CARTS),2001, San Diego, pp. 62-67.
- "Tin Whiskers: Attributes and Mitigation", Proceedings Capacitor and Resistor Technology Symposium (CARTS) EUROPE 2002: 16th Passive Components Symposium, 2002
- "Third Harmonic Testing: Current Resistor Applications, Proceedings Capacitor and Resistor Technology Symposium (CARTS),
- "Tin Whiskers: Attributes and Mitigation", Capacitor and Resistor Technology Symposium 2002 CARTS, 2002
- "ESR Concerns in tantalum chip capacitors exposed to non-oxygen-containing environments" Microelectronics Reliability, 42 , 2002
- "Chip Scale Packaging: A New Look at Reliability Considerations", 2003.
- "Integrating MEMS Quality And Reliability Goals With The Use Of Multi-Valued Logic Analysis", 2003.
- "A Capacitor's Inductance : Critical Property For Certain Applications" , Proceedings Electronic Components Conference, 2004.
- "A Capacitor's Inductance" Proceedings Capacitor and Resistor Technology Symposium (CARTS). 2004.
- "Passive Components in the MEMS and Nanotechnology World - An Overview", Proceedings Capacitor and Resistor Technology Symposium (CARTS). 2004.